CLAIMS

What is claimed is:

1. A method of reducing interference in a circuit having a PLL, wherein the circuit is formed on an integrated circuit, the method comprising the steps of:

providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by a desired amount; and

providing the divider circuit by placing a fixed-value divider at the input of the PLL to reduce the digital current created by the PLL.

2. The method of claim 1, wherein the step of providing a divider circuit further comprises the step of providing first and second dividers connected in series at the input of the PLL, wherein the first and second dividers are fixed-value dividers.

3. The method of claim 2, wherein the one of the dividers divides the input frequency by thirteen and the other divider divides the input frequency by five.

4. The method of claim 1, wherein:

the PLL is powered by a first voltage;

the divider circuit is powered by a second voltage; and

the second voltage is less than the first voltage.

5. A method of reducing interference present in a circuit comprising the step of:

reducing the mutual inductance between digital circuitry in a first portion of the circuit and circuitry in a second portion of the circuit by placing a filter between the

digital circuitry and a voltage source external to the circuit in order to reduce the area of a high frequency current loop.

6. The method of claim 5, wherein the circuit is formed on an integrated circuit, and wherein the first portion of the circuit includes PLL digital circuitry and the second portion includes a VCO.

7. The method of claim 5, wherein the filter is a low pass filter.

8. The method of claim 5, wherein the filter creates a secondary current loop for confining current at a desired frequency in the secondary current loop.

9. The method of claim 8, wherein the filter creates a third current loop for confining current at a desired frequency in the third current loop.

10. The method of claim 5, wherein the filter is provided by placing a capacitor across first and second nodes in the digital circuitry and placing a resistor between the first node and the voltage source.

11. The method of claim 10, wherein the filter is further provided by placing a second capacitor between the second node and the resistor and placing a second resistor between the first resistor and the voltage source.

12. A method of reducing interference present in a circuit formed on an integrated circuit comprising the steps of:

identifying a conductive trace on the circuit carrying high frequency digital current; and

placing a conductive strip in the proximity of the identified conductive trace to help contain the high frequency current flowing through the conductive trace.

13. The method of claim 12, wherein the conductive strip is coupled to a reference voltage at one end.

14. The method of claim 12, wherein the conductive strip has first and second opposite ends, wherein the first end makes a connection to a reference voltage, and wherein the second end makes no connection.

15. The method of claim 12, wherein the conductive strip is substantially parallel to the identified conductive trace.

16. The method of claim 12, further comprising the step of placing a second conductive strip in the proximity of the identified conductive trace.

17. The method of claim 16, further comprising the step of placing a third conductive strip in the proximity of the identified conductive trace.

18. The method of claim 12, wherein the circuit includes PLL and VCO circuitry for use with a wireless communications system.

19. A conduit for shielding a conductive trace carrying high frequency digital current on a circuit formed on an integrated circuit in order to reduce interference present in the circuit, the conduit comprising:

a first conductive strip positioned substantially parallel to the conductive trace; and

a contact connecting the conductive strip to a reference voltage.

20. The conduit of claim 19, wherein the contact is connected to the conductive strip near an end of the conductive strip.

21. The conduit of claim 20, wherein the conductive strip is open at the opposite end.

22. The conduit of claim 19, further comprising a second conductive strip positioned substantially parallel to the conductive trace.

23. The conduit of claim 22, wherein the first and second conductive strips are positioned on opposite sides of the conductive trace.

24. The conduit of claim 19, wherein the circuit is an integrated circuit which includes multiple metal layers, and wherein the conductive trace is formed on one of the metal layers.

25. The conduit of claim 24, wherein the first conductive strip is formed on a first metal layer.

26. The conduit of claim 25, further comprising a second conductive strip formed on a second metal layer.

27. The conduit of claim 26, wherein the first and second conductive strips are electrically connected together.

28. The conduit of claim 27, wherein the first and second conductive strips are connected to the substrate of the integrated circuit.

29. The conduit of claim 19, wherein the integrated circuit includes PLL and VCO circuitry for use with a wireless communications system.

30. A method of reducing interference present in a circuit, the circuit having a plurality of similar circuit elements, the method comprising the step of:
forming at least some of the similar circuit elements on the circuit such that adjacent circuit elements are mirror images of one another.

31. The method of claim 30, wherein the circuit is formed on an integrated circuit having PLL and VCO circuitry for a wireless communications system.

32. The method of claim 30, wherein the circuit elements are flip flops.

33. The method of claim 32, wherein the flip flops form counters for the PLL.

34. A method of reducing interference present in a circuit, the method comprising the steps of:
providing a first block of digital circuitry connected to a second block of digital circuitry by a signal line; and
inserting buffer circuitry between the first and second blocks of digital circuitry for containing high frequency current within the first block of digital circuitry.

35. The method of claim 34, wherein the circuit is formed on an integrated circuit having PLL and VCO circuitry for a wireless communications system.

36. The method of claim 34, wherein the buffer circuitry is formed on an integrated circuit near the location on the integrated circuit where the first block of digital circuitry is formed.

37. The method of claim 34, wherein the signal line is a control line.

38. The method of claim 34, wherein the signal line is a status line.

39. The method of claim 34, wherein the buffer circuitry is comprised of one or more inverters.

40. The method of claim 39, wherein at least one of the inverters is powered by a filtering capacitor coupled to the at least one inverter.

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41. A method of reducing interference present in a circuit formed on an integrated circuit having PLL and VCO circuitry, the method comprising the step of:

identifying circuitry in the circuit in which the impedance of the circuitry changes state over time during operation of the circuit; and

creating replica circuitry of the identified circuitry which operates in a state opposite of the identified circuitry.

42. The method of claim 41, wherein the replicated circuitry has no function in the circuit other than reducing interference.

43. The method of claim 41, wherein the identified circuitry is comprised of a first inverter having a high state and a low state, wherein the replica circuitry is comprised of a second inverter having a high state and a low state, and wherein the replica inverter is controlled to be in the opposite state of the other inverter.

44. The method of claim 41, wherein the replica circuitry is comprised of circuitry similar to the identified circuitry, the method further comprising the step of connecting an inverter between an input of the identified circuitry and an input of the replica circuitry.

45. A filter for filtering an interface pin of integrated circuit having PLL and VCO circuitry to reduce interference caused by signals at the interface pin of the integrated circuit, the filter comprising:

a filter coupled to the interface pin of the integrated circuit.

46. The filter of claim 45, wherein the interface pin is a clock signal input for receiving a clock signal from an external clock source, and wherein the filter isolates the clock signal while allowing the clock signal to pass through to the integrated circuit.

47. The filter of claim 46, wherein the filter is an RC filter.

48. The filter of claim 47, wherein the filter is comprised of a capacitor connected across the interface pin and a second pin of the integrated circuit and a resistor connected between the interface pin and the external clock source.

49. The filter of claim 45, wherein the interface pin is an input, and wherein the integrated circuit includes electrostatic discharge (ESD) circuitry, wherein the ESD circuitry is coupled at a point between the filter and the remainder of the integrated circuit.

50. The filter of claim 45, wherein the interface pin forms an input to the integrated circuit.

51. The filter of claim 45, wherein the interface pin forms an output to the integrated circuit.

52. A method of integrating VCO and PLL circuitry for a wireless communication system onto a single integrated circuit comprising the steps of:

forming an integrated circuit having both PLL circuitry and VCO circuitry integrated on the integrated circuit; and

applying one or more techniques to reduce interference present near the frequency of an output of the VCO.

53. The method of claim 52, wherein the one or more techniques includes providing fixed divider circuitry for the PLL.

54. The method of claim 53, wherein the divider circuitry further comprises first and second series connected fixed dividers.

55. The method of claim 52, wherein the one or more techniques includes reducing the mutual inductance between digital circuitry in the PLL and the VCO circuitry by placing a filter between digital circuitry in the PLL and a voltage source external to the integrated circuit in order to reduce the area of a high frequency current loop.

56. The method of claim 52, wherein the one of the one or more techniques includes:
identifying a conductive trace on the integrated circuit carrying high frequency digital current; and
placing a conductive strip in the proximity of the identified conductive trace to help contain the high frequency digital current flowing through the conductive trace.

57. The method of claim 52, wherein the integrated circuit includes a plurality of similar circuit elements, and wherein one of the one or more techniques includes forming at least some of the similar circuit elements on the integrated circuit such that adjacent circuit elements are mirror images of one another.

58. The method of claim 52, wherein one of the one or more techniques includes providing a first block of digital circuitry connected to a second block of digital circuitry by a signal line, and inserting buffer circuitry between the first and second blocks of digital circuitry for containing high frequency current within the first block of digital circuitry.

59. The method of claim 52, wherein one of the one or more techniques includes the steps of:

identifying circuitry in the integrated circuit in which the impedance of the circuitry changes over time during operation of the integrated circuit; and

creating replica circuitry of the identified circuitry which operates in a phase opposite of the identified circuitry.

60. The method of claim 52, wherein the integrated circuit includes an interface pin, wherein one of the one or more techniques includes the step of:

providing a filter coupled to the interface pin of the integrated circuit to reduce interference caused by signals at the interface pin.

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